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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,776	02/11/2002	Richard J. Manzolati	D/A0A46 (1508/3530)	2022

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EXAMINER	
STEELMAN, MARY J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,776	MANZOLATI, RICHARD J.	
	Examiner	Art Unit	
	Mary J. Steelman	2122	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/11/2002, 5/13/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/14/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are pending.

Information Disclosure Statement

2. IDS received 14 May 2004 has been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being unpatentable over US Patent 6,353,841 to Marshall et al.

Per claims 1 and 8:

-obtaining information about at least one part of an apparatus;

(FIG. 9, col. 15, lines 32-36, "Input signals containing dynamic instructions...are received (obtaining information) from connections...")

-determining instructions for optimizing at least one operation of the apparatus based on the obtained information;

(Col. 15, lines 45-50, "The signals input from the wiring network pass through a dynamic instruction enable gate. The function of this gate is to enable either dynamic instruction bits...or to prevent them from being used (determine enable or disable)...This is determined by a single bit of configuration RAM for that ALU..."

-applying the instructions to the at least one operation of the apparatus.

(Col. 15, lines 50-55, "If the dynamic instruction bits are to be used, gate passes the values of I input from the wiring network (applying instructions). If not, then the output of gate will be zero, and the instruction input to the ALU will be that which has already been stored as stored instruction...")

Per claim 15:

An apparatus comprising:

-one or more parts;

(FIGs. 1 & 2 – shows multiple parts.)

-an information component for at least one of the part, the information component having data about the at least one part;

(Col. 6, lines 1-8, "...each ALU has a first pair of 4-bit inputs a, which are directly connected within the ALU, a second pair of 4-bit inputs b...and four 4-bit outputs f...Each ALU also has an independent pair of 1-bit carry inputs..." multiple parts with information)

-an optimization processing system that determines instructions for optimizing at least one operation of the apparatus based on the data and applies the instructions to the at least one operation of the apparatus to optimize the performance.

(Col. 4, lines 31-37, "To allow an individual device to accept or reject dynamic instructions, it is desirable to provide for each of the processing devices a dynamic enable gate to determine whether instructions to determine the function of the arithmetic logic unit are to be accepted dynamically from the interconnect or are to be provided from configuration memory (optimize performance)...")

Per claims 2, 9, and 16:

-identifying the at least one operation of the apparatus being optimized, wherein the obtaining information obtains the information from the at least one part involved in the at least one identified operation.

(Col. 4, lines 39-43, "...application of the dynamic instruction mask (identify instruction) to an instruction received by the processing device enables the instruction to provide both an instruction input to the arithmetic logic unit for determining the function of the arithmetic logic unit...")

Per claim 3, 10, and 17:

-interrogating the at least one part for the information.

(Col. 4, lines 39-43, "...application of the dynamic instruction mask to an instruction received by the processing device enables the instruction to provide both an instruction input to the

arithmetic logic unit for determining the function of the arithmetic logic unit (interrogate part)...")

Per claims 4, 11, and 18:

-determining if any other parts need to be interrogated;

(FIG. 1 – indicates 6 ALUs, each of which may be interrogated. Col. 4, lines 39-43, "...application of the dynamic instruction mask to an instruction received by the processing device enables the instruction to provide both an instruction input to the arithmetic logic unit for determining the function of the arithmetic logic unit...")

-interrogating the other parts which are needed for the obtained information.

See rejection of claims 3 and 4 above. Multiple parts are interrogated for information.

Per claims 5, 12, and 19:

-obtained information for the at least one of the part comprises at least one functional parameter of the at least one part.

(Col. 9, lines 13-16, "Accordingly only when the ENABLE signal is high and the content of the memory cell is high (parameter), the conductor...are connected ...", col. 10, lines 8-10, "...using the properties of memory cell. Both the content and the complement of the content of this memory cell are readily available as outputs.")

Per claims 6, 13, and 20:

-obtained information for the at least one of the part comprises at least one algorithm of the at least one part.

(Col. 10, lines 38-41, "Appropriate construction and connection of multiplexer...allows selection of a value received from the wiring network as the output of the multiplexer or buffer...with that value then being used in determining the instruction of the ALU..." , col. 10, lines 46-48, "Use of the multiplexer or buffer for this purpose means that the value used for providing instruction to the ALU (algorithm) is also the value made available for passing onwards...")

Per claims 7, 14, and 21:

-comparing the obtained information about the at least one part against stored information about the at least one part to obtain a difference;

(Col. 14, Table 3 – AEQUALSB, MATCH1, MATCH0: Compare operators are disclosed.)

-using the difference to determine the instructions for optimizing the at least one operation of the apparatus.

(Col. 15, lines 21-22, "...ability to generate an instruction for a functional unit as the output of another functional unit.")

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached at (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman

11/17/2004

WEI Y. ZHEN
PRIMARY EXAMINER